

## REMARKS

Claims 1, 4-10, 13-17, and 20 are presently pending and stand rejected. Continued Examination is respectfully requested.

Claim 1, 9, and 17 were rejected under 35 U.S.C. 103(a) as being obvious from the combination of Jones in view of Gelsomini. Claim 20 was rejected as being obvious from the combination of Jones, Gelsomini, and Khoury.

Claim 1 is amended to recite, among other limitations, “determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element”.

Assignee respectfully submits that the combination Jones and Gelsomini does not teach “determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element”. Examiner has indicated that Jones teaches “determining if the state of the element (DR0 in Fig. 3b) is equal to an expected state (VERIFY DATA 0 in Fig. 3b) using a verify circuit (308 in Fig. 3a)”. Compare logic 308 is further illustrated in Fig. 3b, which shows exclusive OR (XOR) gate 380 comparing the data shift register bit zero (DR0) with the verify data bit zero [VERIFY DATA 0].” Col. 4, Lines 11-14. Since Jones shows an “exclusive OR (XOR) gate 380 comparing”, it is respectfully submitted that Jones does not teach “determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element”.

Examiner has indicated that it would have been obvious at the time of the invention to “substitute a thin oxide gated fuse having an oxide that is less than 2.5 nm thick for the memory element of Jones”. Even if the “thin oxide gated fuse” was substituted with the memory element, Assignee respectfully submits that the combination would not teach or fairly suggest “determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element”. This is because the “exclusive OR (XOR) gate 380” does not compare or determine “electrical resistance”.

Additionally, claims 9, and 17 are amended to recite, among other limitations, “wherein the state is a state of electrical resistance”. For the reasons above, Assignee

respectfully submit that the combination of Jones, and Gelsomini do not teach or fairly suggest "wherein the state is a state of electrical resistance". Accordingly, Examiner is requested to withdraw the rejection to claims 9 and 17 as well as to dependent claims 10, and 13-16.

Claim 20 is also amended to recite, among other limitations, wherein the state is a state of electrical resistance". Claim 20 was rejected from the combination of Jones, Gelsomini, and Khoury. Examiner has merely indicated that "Khoury discloses a reference cell". Accordingly, for the foregoing reasons, Assignee respectfully submits that claim 20 is allowable. Accordingly, Examiner is requested to withdraw the rejection to claim 20.

The pending claims were also rejected on the grounds of double patenting. A nonstatutory obviousness type double patenting rejection can be overcome by a timely filed terminal disclaimer. Accordingly, Assignee presents Examiner with a terminal disclaimer and it is respectfully submitted that the foregoing rejection is now overcome.

For at least the foregoing reasons, each of the pending claims are in a condition for allowance. Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017. In view of the foregoing, it is respectfully submitted that the pending claims define allowable subject matter. Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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Mirut Dalal  
Registration No. 44,052  
Attorney for Assignee

January 9, 2008

McAndrews, Held & Malloy, Ltd.  
500 West Madison Street, 34<sup>th</sup> Floor  
Chicago, Illinois 60661

Phone (312) 775-8000  
FAX (312) 775-8100